What is claimed:

1. A method for manufacturing a semiconductor device having a trench element isolation region including a trench and a trench insulating layer that fills the trench, the method comprising the steps of:

(A) forming a polishing stopper layer over a substrate, the polishing stopper layer having a predetermined pattern for a chemical-mechanical polishing;

(B) removing a part of the substrate using a mask layer including at least the polishing stopper layer as a mask to form a trench;

(C) forming a trench oxide film over a surface of the substrate that forms the trench;

(D) forming an insulating layer that fills the trench over an entire surface of the substrate;

(E) polishing the insulating layer by a chemical-mechanical polishing;

(F) removing the polishing stopper layer; and

(G) etching a part of the insulating layer to form a trench insulating layer,

wherein the method further includes the step (a) of forming an etching stopper layer for the trench oxide film over at least a portion of the trench oxide film, and wherein, in the step (G), the etching stopper layer is more resistant to the etching than insulating layer.

2. A method for manufacturing a semiconductor device according to claim 1, wherein, in the step (G), a selective etching ratio of the insulating layer with respect to the etching stopper layer is 10 or greater.

3. A method for manufacturing a semiconductor device according to claim 1, wherein the etching stopper layer is formed to cover a side surface of the trench oxide film.

4. A method for manufacturing a semiconductor device according to claim 1, wherein the etching stopper layer is a silicon nitride layer.

5. A method for manufacturing a semiconductor device according claim 4, wherein the silicon nitride layer has a thickness of 10 – 50 nm.

6. A method for manufacturing a semiconductor device according to claim 1, wherein the etching stopper layer is a non-monocrystal silicon layer.

7. A method for manufacturing a semiconductor device according claim 6, wherein the non-monocrystal silicon layer is selected from the group consisting of a polycrystal silicon layer, an amorphous silicon layer or a multiple layer having a polycrystal silicon layer and an amorphous silicon layer.

8. A method for manufacturing a semiconductor device according claim 6, wherein the non-monocrystal silicon layer has a thickness of 20 – 50 nm.

9. A method for manufacturing a semiconductor device according to claim 6, further comprising, after the step (G), the step (b) of thermally oxidizing a portion of the non-monocrystal layer that protrudes from the surface of the substrate in an element forming region to form a silicon oxide film.

10. A method for manufacturing a semiconductor device according claim 9, wherein the silicon oxide film is removed at the same time as the step (G).

11. A semiconductor device comprising trench element isolation regions, wherein at least one of the trench element isolation regions includes a trench oxide film formed on a surface of a substrate that forms a trench, and a trench insulating layer formed in the trench, wherein an etching stopper layer is formed such that a surface of the trench oxide film on a side wherein the trench insulating layer is formed is not exposed.

12. A semiconductor device comprising trench element isolation regions, wherein at least one of the trench element isolation regions comprises:

a trench oxide film formed on a surface of a substrate that forms a trench,

a trench insulating layer formed in the trench, and

an etching stopper layer formed between the trench oxide film and the trench insulating layer.

13. A semiconductor device according to claim 12, wherein the etching stopper layer is formed from a material having a selective etching ratio of the insulating layer to the etching stopper layer of at least ten (10) when an etchant including hydrofluoric acid is used.

14. A semiconductor device according to claim 12, wherein the etching stopper layer is formed on a surface of the trench oxide film.

15. A semiconductor device according to claim 12, wherein the etching stopper layer comprises a silicon nitride layer.

16. A semiconductor device according to claim 12, wherein the etching stopper layer is a silicon nitride layer having a thickness of 10 – 50 nm.

17. A semiconductor device according to claim 12, wherein the etching stopper layer comprises a non-monocrystal silicon layer.

18. A semiconductor device according to claim 12, wherein the etching stopper layer is a non-monocrystal silicon layer having a thickness of 20 – 50 nm.

19. A semiconductor device according to claim 18, wherein the non-monocrystal silicon layer is selected from the group consisting of a polycrystal silicon layer, an amorphous silicon layer or a multiple layer having a polycrystal silicon layer and an amorphous silicon layer.

20. A semiconductor device according to claim 11, wherein the etching stopper layer is formed from a material having a selective etching ratio of the insulating layer to the etching stopper layer of at least ten (10) when an etchant including hydrofluoric acid is used.

21. A semiconductor device according to claim 11, wherein the etching stopper layer comprises a silicon nitride layer.

22. A semiconductor device according to claim 11, wherein the etching stopper layer is a silicon nitride layer having a thickness of 10 – 50 nm.

23. A semiconductor device according to claim 11, wherein the etching stopper layer comprises a non-monocrystal silicon layer.

24. A semiconductor device according to claim 11, wherein the etching stopper layer is a non-monocrystal silicon layer having a thickness of 20 – 50 nm.

25. A semiconductor device according to claim 24, wherein the non-monocrystal silicon layer is selected from the group consisting of a polycrystal silicon layer, an amorphous silicon layer or a multiple layer having a polycrystal silicon layer and an amorphous silicon layer.

26. A method for manufacturing a semiconductor device, comprising:

forming a trench comprising a lower surface and two side surfaces in a substrate comprising silicon;

forming a trench oxide layer on the lower surface and side surfaces;

forming an etch stop layer in direct contact with the trench oxide layer on the lower surface and side surfaces;

filling the trench with an insulating layer directly contacting the etch stop layer, wherein the insulating layer overfills the trench and extends above the trench as defined by the two side surfaces; and

etching the insulating layer using an etchant that selectively etches the etch stop layer at a rate that is slower than that of the insulating layer.